

Observation of Tunneling Current in Semiconducting Graphene p - n Junctions

Hisao Miyazaki,^{*} Michael Lee, Song-Lin Li, Hidefumi Hiura,[†] and Kazuhito Tsukagoshi[‡]

MANA, National Institute for Materials Science, Namiki, Tsukuba 305-0047, Japan

Akinobu Kanda^{*}

Institute of Physics, University of Tsukuba, Tsukuba 305-8571, Japan

(Dated: November 16, 2011)

We demonstrate a tunneling and rectification behavior in bilayer graphene. A stepped dielectric top gate creates a spatially modulated electric field, which opens the band gap in the graphene and produces an insulating region at the p - n interface. A current-voltage relationship exhibiting differential resistance peak at forward bias stems from the tunneling current through the insulating region at the p - n interface. The tunneling current reflects singularities in the density of states modified by the electric field. This work suggests that the effect of carrier charge tuning by external electric field in 2D semiconductors is analogously to that by impurity doping in 3D semiconductors.

Keywords: bilayer graphene, field effect, p - n junction, tunneling effect

I. INTRODUCTION

In an atomically-thin two-dimensional (2D) conductor like graphene, carrier charges can be induced with an external electric field[1]. Inducing carrier charges by an electric field is one significant advantage of 2D conductors, because it provides uniformly distributed carrier charges and overcomes the problem of random spatial fluctuation of dopants[2]. This random fluctuation is one of the important problems in nanoelectronics that use traditional

^{*}CREST, Japan Science and Technology Agency, Kawaguchi 332-0012, Japan

[†]NEC Corporation, Tsukuba 305-8501, Japan

[‡]CREST, Japan Science and Technology Agency, Kawaguchi 332-0012, Japan; Electronic address: TSUKAGOSHI.Kazuhito@nims.go.jp

intrinsic semiconductors. A top gate that induces distinct localized electric fields in the 2D conductor can produce distinct regions with different carriers, thus forming a p - n junction in graphene that are required for devices[3, 4]. Klein tunneling[5, 6] and quantum Hall edge modes[7, 8] have been observed in these junctions. In monolayer graphene, such gate-controlled p - n junctions have been demonstrated increase the resistance through the active regions. However, an efficient barrier to current flow that will produce diode current-voltage characteristics has not yet been reported. An efficient barrier requires a potential barrier region to be induced in a 2D conductor with a bandgap.

In this paper, we report the realization of such a barrier region at a p - n junction in bilayer graphene (BLG), the first observation of tunneling through a p - n junction induced by electric fields in semiconducting BLG, and the first instance of rectification in a device based on a 2D material. We observed a differential resistance peak at forward source-drain bias. We attribute this peak to tunneling between p and n regions, and credit it for diode behavior similar to what is observed in a 3D Esaki diode[9–11]. We employed a uniform bottom gate and a stepwise top gate to form a p - n interface. A thin top gate dielectric (less than 10 nm) [12] is critical to shrink the spatial transition between p and n regions. The electric field between the top gate and the bottom gate opens a band gap in the BLG[13–18], making a tunnel barrier between p and n regions. As this is the first instance of rectification in 2D, we anticipate our approach will provide a starting point for creating gate-controlled diodes in 2D conductors. Furthermore, a gate-controlled p - n junction would be utilized in optoelectronic devices operating in the THz regime[19, 20], which is covered by the gate-tunable range of the band gap in BLG. Utilizing the tunneling effect has an advantage for high speed electronics which would be one major application area for graphene electronics[21].

II. EXPERIMENTAL APPROACH

An electric field produced by a stepped-gate can generate opposing charges under each half of the gate (Fig. 1(a)). A charge-neutral region exists under the step. If the 2D semiconductor has a band gap, charge carriers are depleted in the charge-neutral region. The depletion region has an in-plane electric field which originates from the gate electric field, canceled partially by the electric field from charge carriers in the 2D semiconductor. This mechanism sharply contrasts the impurity-doped p - n junction in a 3D semiconductor,

where carrier recombination produces a depletion region. The depletion of carriers leaves charged donor and acceptor impurities, resulting in a built-in electric field[9]. We note that the charge-neutral region and charged region in the gate-controlled p - n junction is opposite from the impurity-doped one: In the gate-controlled one, the depletion region is charge-neutral, while p and n regions are charged by carriers. In the impurity-doped one, the depletion region is charged by dopants (donors and acceptors), and uniform regions are charge-neutral. In spite of these differences, a model based on electrostatics suggests that the gate-controlled p - n junction in 2D mirrors the operation of the impurity-doped one in 3D (Appendix A).

III. SAMPLE FABRICATION

BLG samples were prepared from kish graphite by the mechanical cleavage method[1] and adhered on to a highly-doped Si substrate with a 90-nm-thick SiO_2 surface layer. A graphene sample with multiple electrodes was patterned by oxygen plasma etching for four-terminal measurements (Fig. 1(b)). The bilayer channel was $0.4\ \mu\text{m}$ in width and was sandwiched between a substrate bottom gate and a stepped top gate. The top gate was composed of two regions with different gate dielectric thicknesses. Half of the area of the graphene channel (surrounded by dashed lines in Fig. 1(b)) was covered by a 5-nm-thick layer of SiO_2 . Then, the entire area of the graphene between the voltage terminals was covered by a 30-nm-thick Al film. The sample was exposed to air for several hours for partial oxidization of the Al film. An oxidized (AlO_x) layer formed not only on the surface but also at the interfaces of Al/graphene[18, 22, 23] and Al/ SiO_2 [24, 25]. The SiO_2 layer between part of the graphene and the AlO_x layer, increases the dielectric thickness over that region[26] which results in the formation of a stepwise junction in the top gate (Fig. 1(c)). When a voltage is applied to the top gate, two different electric fields are simultaneously applied to the individual regions. The field effect mobilities extracted from the gate voltage dependence were $1300\ \text{cm}^{-2}\text{V}^{-1}\text{sec}^{-1}$ for electrons and $1800\ \text{cm}^{-2}\text{V}^{-1}\text{sec}^{-1}$ for holes, independent of the dielectric thickness.

IV. RESULTS AND DISCUSSION

The two gate regions with different dielectrics thicknesses create charge neutrality point (CNP) ridges with different slopes in the $V_{\text{bg}}\text{-}V_{\text{tg}}$ plane. Figure 1(d) shows a contour plot of the resistance R_0 through the junction as a function of V_{bg} and V_{tg} . The two ridges separate the $V_{\text{bg}}\text{-}V_{\text{tg}}$ plane into $p\text{-}p$, $p\text{-}n$, $n\text{-}p$, or $n\text{-}n$ combinations of carrier polarity in the graphene. On the ridge of CNPs, the height of the resistance peak increased with an increasingly negative electric field ($V_{\text{bg}} \rightarrow -40$ V) as an evidence of the band gap opening under the electric field[18]. From the slope of the CNP lines, we can extract the top gate capacitance values[3]: $C_{\text{tg1}} = 9.3 \times 10^{-3}$ F/m² in the thick region and $C_{\text{tg2}} = 5.5 \times 10^{-3}$ F/m² in the thin region. If we assume the dielectric film is simply composed of SiO₂, equivalent thicknesses are approximately 3.7 nm ($= d_1$) and 6.3 nm ($= d_2$), respectively. The stepwise top gate causes a transient region of ~ 5 nm which gives a width of the insulating region W_{D} (Fig. 1(e) and Appendix A).

In an actual bilayer of graphene with a band gap, a disordered potential forms a band tail[27]. The band structure forms two peaks in the density of states (DOS) at the edge of the valence band and the conduction band[28, 29]. The energy gap between the two peaks E_g hardly depends on disorder, and is almost identical to the band gap in the unperturbed system[30]. This gap can be extracted from the temperature dependence of the conductance at the CNP[18]. The CNP conductance comprises the intrinsic band conduction and the hopping conduction via localized states which make up the band tail. The former has a thermal activation energy $E_g/2$. Extracted E_g is ~ 0.2 eV at $V_{\text{bg}} = -40$ V both in the thin and thick dielectric region. The band gap makes an insulating region inserted between the p and n regions. Using this band gap, we estimate tunneling probability across the junction to be 0.07 and the tunnel resistance R_t to be several k Ω (Appendix B). The hopping conduction causes leakage current coexisting with the tunnel conduction. The leakage resistance is estimated to be $R_L \sim 1$ k Ω (Appendix B), which is comparable to the tunnel resistance. Then, the junction resistance, $R_j = 1/(1/R_t + 1/R_L)$, is on the order of 1 k Ω . Using this value, it is estimated that the voltage drop at the junction V_j is a few percent of V_{ds} .

The differential resistance dV_{ds}/dI was measured in a four-terminal configuration across the $p\text{-}n$ junction as a function of the source-drain voltage V_{ds} , rather than the leakage current, to investigate the junction property because the differential resistance is sensitive

to a nonlinear tunneling current. We found a dV_{ds}/dI peak for a large bottom gate voltage ($V_{bg} = -40$ V) that opens the band gap (Fig. 2(a)). The peak was not observed for a bottom gate voltage ($V_{bg} = -32$ V) that was too small to open the band gap (bottom-right inset of Fig. 2(a)). The increase of the dV_{ds}/dI at large V_{ds} is caused by charge redistribution by the V_{ds} bias[31]. The peak appeared at a forward bias of $V_{ds} \sim 50$ mV, regardless of V_{bg} or V_{tg} (Fig. 2(b)). The peak height depends on the bottom gate voltage and became pronounced when the gate electric field was increased by applying V_{bg} (Fig. 2(c)).

We analyze the dV_{ds}/dI peak observed in the experiment. A DOS diagram of the unbiased p - n junction is illustrated in Fig. 3(a)i). The voltage drop, V_j , depresses the energy in the p -type side (Fig. 3(a)ii). The tunneling current, I_t , from the p to n region is given by $I_t \propto T_t \int [f(E - E_F) - f(E - E_F + eV_j)] D_n(E) D_p(E + eV_j) dE$, where $f(x) = 1/[\exp(x/k_B T) + 1]$ is the Fermi distribution function, and $D_p(\varepsilon)$ and $D_n(\varepsilon)$ are the DOS at the energy level ε (measured from the mid-gap) for the p -type and n -type sides[9]. The tunneling current reaches a maximum when the peaks in $D_p(E + eV_j)$ and $D_n(E)$ align at the energy level (Fig. 3(a)ii). For a larger V_j , the tunneling current becomes smaller because the DOS peaks go out of alignment (Fig. 3(a)iii). As a result, the tunneling current has a peak that is a function of V_{ds} . In the total current, the tunneling current becomes indistinguishable from the leakage current via localized states when the leakage current is comparable to or larger than the tunneling current. The peak structure displayed a dV_{ds}/dI peak, as shown in Fig. 3(b), which was observed at $V_{ds} \sim 50$ mV. Because the voltage drop at the junction is a few percent of V_{ds} , the energy difference between the Fermi level and the band edge must be on the order of a few meV.

The temperature dependence of the dV_{ds}/dI peak (Fig. 4(a)) gives reasonable support to the model of the tunnel junction discussed above. Using the Sommerfeld expansion in terms of temperature[32], the tunneling current is proportional to $T_t \int_{E_F - eV_j}^{E_F} [P(E) + a_1 (k_B T)^2 P''(E)] dE$ within the second order of the temperature T , where $P(E) = D_n(E) D_p(E + eV_j)$, $P''(E) = d^2 P(E)/dE^2$, and $a_1 = \frac{1}{2} \int_{-\infty}^{\infty} x^2 \left(-\frac{d}{dx} \frac{1}{\exp(x)+1} \right) dx \sim 1.6$. The function $P(E)$ represents a density of states for elastic tunneling between the p and n region. Because a temperature coefficient for the second order is proportional to the integration of $P''(E)$ around the Fermi level, a trend of the tunneling current in the temperature dependence is determined by convex upward or downward in the $P(E)$. For a peak in tunneling current, $P(E)$ has a peak around the Fermi level, i.e. $P''(E_F) < 0$ (Fig.

4(b)). Thus, the tunneling current decreases with increasing T . This trend can be observed in the temperature dependence of dV_{ds}/dI - V_{ds} , as shown in Fig. 4(a); the decrease in the tunneling current peak causes the dV_{ds}/dI peak to diminish as the temperature increases (Fig. 4(c)). The decrease in the tunneling current peak also leads to the V_{ds} dependence in the dV_{ds}/dI - T curve (Fig. 4(d)). At a low V_{ds} bias ($V_{\text{ds}} = 0$), dV_{ds}/dI becomes larger at higher temperatures, reflecting the decrease in the tunneling current. In contrast, at higher V_{ds} bias voltages, dV_{ds}/dI becomes smaller at higher temperatures, reflecting the decrease in the dV_{ds}/dI peak (Fig. 4(c)). Here, a second-order temperature coefficient ($1.3 \times 10^{-5} \text{ K}^{-2}$) is extracted from the dV_{ds}/dI - T curve at the dV_{ds}/dI maximum ($V_{\text{ds}} = 50 \text{ mV}$). A corresponding energy for the temperature coefficient is 20 meV. Because the temperature coefficient ($\propto P''(E_{\text{F}})$) determines the sharpness of the $P(E)$ peak, the corresponding energy represents a broadness of the peak, caused by band tail of the DOS. This indicates that the band tail width is approximately 20 meV which on the order of 10% of the energy gap E_{g} .

The thermal energy at higher temperatures also generates a leakage current via localized states. The leakage current becomes larger with higher T , while the tunneling current becomes smaller. The tunneling current is more dominant than the leakage current in the temperature dependence, because the dV_{ds}/dI at $V_{\text{ds}} = 0$ becomes larger at higher temperature. The overall trend of the dV_{ds}/dI peak observed in this experiment is similar to the negative differential resistance (NDR) of the Esaki diode[9–11]. For a larger NDR in graphene, the leakage current must be suppressed. The impurity states in the band gap under high electric field are the most probable cause of the leakage current. Thus, reducing impurities and defects is important for fabricating a diode device governed only by the tunneling effect.

V. CONCLUSIONS

We observed clear tunneling signals in semiconducting BLG p - n junctions. This provides the first experimental evidence for the existence of conduction barrier in gap tunable atomic-layer conductors, which is essential to realize wavelength-tunable optoelectronic devices. We also identified localized states as the source of the diffusion current within the band gap, which highlights the importance to exclude the impurities and disorder in graphene to improve performance. With appropriate biasing conditions and transparent top gate stacks

for THz electromagnetic waves, novel wavelength-tunable optoelectronic devices would be viable in BLG.

Acknowledgments

This work was supported in part by KAKENHI (No. 21241038) from the MEXT of Japan and by the FIRST Program from the JSPS. The authors would like to thank S. Okada, M. Otani, M. Koshino, and K. Wakabayashi for useful discussions. We also thank Covalent Materials Corporation for providing Kish graphite as the source material of graphene.

Appendix A: Width of the Depletion Region

We derive a Poisson equation to describe the electric potential profile in a double-gated 2D semiconductor. Here, we define a 2D conductor as a thin conductor which is much thinner than electric field screening length. Monolayer and bilayer graphene fit to the definition [22]. In the 2D semiconductor, the charge distribution along the thickness direction is negligible. The 2D semiconductor (thickness d_s , dielectric constant ε_s) is sandwiched between a bottom gate and a top gate (Fig. A.1(a)). We consider a small region in the semiconductor from a position x to a position $x + \Delta x$. Gauss's law gives a relationship among the top gate electric field (E_t), the bottom gate electric field (E_b), the electric field in the semiconductor plane (E_i), and charge density in the small region $q(x)$: $\varepsilon_s (E_i(x + \Delta x) - E_i(x)) d_s + (\varepsilon_t E_t - \varepsilon_b E_b) \Delta x = q(x) \Delta x$, with ε_t and ε_b as the dielectric constant of the top gate insulator and the bottom gate insulator, respectively. Taking the limit as Δx approaches zero, we have a one-dimensional Poisson equation for the electric potential (Ψ) in the 2D semiconductor,

$$\frac{d^2 \Psi}{dx^2} = -\frac{dE_i}{dx} = \frac{\varepsilon_t E_t - \varepsilon_b E_b - q(x)}{\varepsilon_s d_s}. \quad (\text{A1})$$

Here, we assume that the top gate electric field is changed abruptly at the junction, such as $E_t = E_{tn}$ for $x \leq 0$ and $E_t = E_{tp}$ for $x > 0$ (abrupt junction). The Ψ is constant in homogeneous regions which are sufficiently distant from $x = 0$. In these regions, the electric field in the semiconductor is zero ($E_i = -d\Psi/dx = 0$), and the charge density is homogeneous ($q(x) = \varepsilon_t E_t - \varepsilon_b E_b$). A p - n junction is formed at $x = 0$ for $eN_p \equiv \varepsilon_t E_{tp} - \varepsilon_b E_b > 0$ and $-eN_n \equiv \varepsilon_t E_{tn} - \varepsilon_b E_b < 0$. There is a transient region from p to

n around $x = 0$. If the 2D conductor has the band gap, charge carriers are depleted from the transient region. Assuming that $|q(x)|$ is much smaller than eN_p and eN_n , the Poisson equation in the depletion region becomes,

$$\begin{aligned} \frac{d^2 \Psi}{dx^2} &= \frac{eN_p}{\varepsilon_s d_s} \quad (\text{for the } p \text{ side}), \\ -\frac{d^2 \Psi}{dx^2} &= \frac{eN_n}{\varepsilon_s d_s} \quad (\text{for the } n \text{ side}). \end{aligned}$$

These equations have same form as in a 3D p - n junction[9], in which the acceptor density (N_A) and the donor density (N_D) are replaced by N_p/d_s and N_n/d_s , respectively. Use the same solution method for the 3D case, we obtain a depletion region width for the abrupt junction,

$$W_D^{\text{abrupt}} = \sqrt{\frac{2\varepsilon_s d_s}{e} \frac{N_p + N_n}{N_p N_n} \Delta \Psi},$$

where $\Delta \Psi$ is the electrical potential difference between the p side and the n side. Using typical values in our experiment ($N_p \sim N_n \sim 2 \times 10^{12} \text{ cm}^{-2}$, $\varepsilon_s = 3.0\varepsilon_0$ for graphite[33], $d_s = 0.67 \text{ nm}$ for bilayer graphene, and $\Delta \Psi \sim E_g = 0.2 \text{ eV}$), the transient region width is $W_D^{\text{abrupt}} \sim 2 \text{ nm}$.

The abrupt junction model is applicable only when the transient region, in which the top gate electric field changes from E_{tn} to E_{tp} , is narrower than the W_D^{abrupt} . If not, we have to take the transient region width as the depletion region width W_D [9]. In the stepwise top gate, the top-gate dielectric thickness is changed from d_1 to d_2 ($d_1 < d_2$) at position $x = 0$ (thick solid line in Fig. A·2(a)). An electric potential, $\phi(x, z)$, between graphene and the top gate is obtained by solving a Poisson equation numerically with a boundary condition, $\phi = 0$ at the graphene ($z = 0$) and $\phi = 1$ at the top gate ($z = d_1$ for $x \leq 0$, and $z = d_2$ for $x > 0$) (Fig. A·2(a)). In the calculation, SiO_2 -equivalent thickness of the dielectric layer ($d_1 = 3.7 \text{ nm}$ and $d_2 = 6.3 \text{ nm}$) is used. The electric field component normal to the graphene, $E_\perp \propto -\partial\phi/\partial z|_{z=0}$, changes with a 5-nm-wide transient region around $x = 0$ (Fig. A·2(b)). In the transient region, the electric field has a tangent component to the graphene, $E_\parallel \propto -\partial\phi/\partial x$, at the vicinity of the graphene surface (Fig. A·2(c)). Since the transient region is wider than the $W_D^{\text{abrupt}} (\sim 2 \text{ nm})$, the transient region width gives the depletion region width, i.e., $W_D \sim 5 \text{ nm}$.

Appendix B: Estimation of Band Diagram and Junction Resistance

Equation (A.1) gives the charge density $q(x)$ in graphene sandwiched by top and bottom gates, $q(x) = \varepsilon_t E_t - \varepsilon_b E_b + \varepsilon_s d_s dE_i/dx$. The gate electric fields are proportional the gate voltages, giving $q(x) = -C_{tg}(x)V_{tg} - C_{bg}V_{bg} + \varepsilon_s d_s dE_i/dx + q_0$ with $C_{tg(bg)}$ as local capacitance for the top (bottom) gate and q_0 as the charge density for $V_{bg} = V_{tg} = 0$. Three typical band diagrams for graphene with spatially modulated charge density are mentioned in Fig. B.1(a)-1(c), corresponding to p - p , n - p , and n - n combinations. In the resistance measurement, these combinations are separated by the two ridges of CNP (Fig. B.1(d)). On the CNPs, the Fermi level is at the mid-gap of the right or left side in the stepwise modulation.

For the V_{tg} fixed in between the two CNPs, a spatial modulation forming a junction with p - and n -region is generated. When the V_{bg} is applied to the p - n junction, the p - and the n -region are separated by the tunneling barrier caused by the band gap (Fig. B.1(b)). The charge density in each p - (or n -) region is given by $q_{p(or\ n)} = -C_{tg}(V_{tg} - V_{CN}^{p(or\ n)})$, where $V_{CN}^{p(or\ n)}$ is the top gate voltage for the CNP in the $p(or\ n)$ -region. When the $V_{bg} = -40$ V and $V_{tg} = 1.0$ V (corresponding to “(b)” in Fig. B.1(d)) are applied, $q_p/e = 1.7 \times 10^{12}$ cm $^{-2}$ (or $q_n/e = 2.5 \times 10^{12}$ cm $^{-2}$) is extracted from $V_{CN}^p = 1.5$ V (or $V_{CN}^n = 0.57$ V). The carrier density $q_{p(or\ n)}/e$ equals to integration of the density of states (DOS) from the mid-gap to the Fermi level. The typical charge density $q_p/e \sim q_n/e \sim 2 \times 10^{12}$ cm $^{-2}$ in our experiment is similar to that in reported experiments on graphene p - n junction [3, 4].

An ideal DOS (D) without band tail is given as a function of the energy (ε) measured from the mid-gap: $D(\varepsilon) \sim (t_\perp/c^2)\sqrt{\Delta/|\varepsilon - E_g/2|}$ for $|\varepsilon| > E_g/2$ and $D(\varepsilon) = 0$ for $|\varepsilon| \leq E_g/2$, with Δ as the potential difference between the two graphene layers and $c(\sim 1 \times 10^6$ m/s) is the Dirac velocity in graphene [29]. The Δ is related to the potential difference between the two graphene layers by $E_g = 2(\Delta - \Delta^3/t_\perp^2)$, where $t_\perp(\sim 0.3$ eV) is the interlayer hopping integral[34], giving $\Delta \sim 0.12$ eV for $E_g \sim 0.2$ eV. Because the DOS of the graphene has a singularity at the band edges ($\varepsilon = \pm E_g/2$) [28, 29], the Fermi level E_p (or E_n) measured from the band edge of the p - (or n -) region is related to the charge density q_p (or q_n) as $q_i/e = -\int_0^{\alpha_i(E_g/2+E_i)} D(\varepsilon)d\varepsilon = -\alpha_i(2t_\perp/c^2)\sqrt{\Delta \cdot E_i}$ ($i = p$ or n), where $\alpha_p = -1$ and $\alpha_n = 1$. Using typical values of the carrier density of $q_p/e = q_n/e \sim 2 \times 10^{12}$ cm $^{-2}$ with potential difference between the two layers $\Delta \sim 0.12$ eV and $E_g = 0.2$ eV in our experiment, the Fermi level of the E_p and E_n in the each side of p - n junction are a few meV. These values

are two orders smaller than the energy gap E_g , indicating that the E_p and the E_n are very close to the singularity peak in the each regions. In a realistic semiconductor graphene with band tails caused by localized states, the singularity peak becomes broader with increasing the density of localized states [28, 29]. Except for the graphene extremely disordered, the E_p and E_n are still much smaller than the E_g , and are close to the band edges. Thus, the band diagram measured in the p - n junction can be described as Fig. B.1(b).

The magnitude of the junction resistance can be roughly estimated from the band diagram. The junction resistance consists of a parallel combination of a tunnel component and a leakage component. The tunnel component is estimated by the tunneling probability of an electron at the junction and the number of states involved in the tunneling. At the junction, the potential gradient is $F \sim E_g/W_D \sim 0.04$ eV/nm, which leads to a tunneling probability across the junction of $T_t = \exp \left[-4\sqrt{2m^*}E_g^{3/2}/(3\hbar F) \right] \sim 0.07$, where $m^* = t_\perp^2/4\Delta c^2 \sim 0.03m_e$ for $\Delta = 0.12$ eV, m_e is the bare electron mass, and $c \sim 1 \times 10^6$ m/s is the Dirac velocity in graphene, for low energy states in a “Mexican hat” band structure[9, 13, 29, 34]. Landauers formula gives the tunnel conductance $1/R_t \sim N(e^2/\pi\hbar)T_t$, where N is the number of quantized wavenumber states in the channel-width direction and \hbar is Planck’s constant. Even at the band edge, the Mexican hat band structure has a non-zero wavenumber range from 0 to k_0 , where $k_0 = \Delta/\hbar c$ (~ 0.2 nm⁻¹ for $\Delta = 0.12$ eV)[13, 34]. The range of the wavenumber in the p -type and n -type region is approximately 0 to k_0 , because the Fermi level is close to the band edge. N is roughly $k_0W/\pi \sim 30$ ($W \sim 0.4$ μ m is the channel width) because the wavenumber is quantized[35] by π/W . Thus, the tunnel resistance R_t is estimated to be several k Ω . The leakage conduction via localized states coexists with the tunnel conduction. The leakage resistance is expressed as $R_L \sim \rho_0 W_D$, where ρ_0 is the residual resistance at the mid-gap states; that is, the resistance per unit length at the CNP. Using $\rho_0 \sim 0.2$ k Ω /nm for $V_{bg} = -40$ V, the leakage resistance is on the order of $R_L \sim 1$ k Ω . Thus, the leakage current is comparable to the tunneling current. Finally, the junction resistance obtained, $R_j = 1/(1/R_t + 1/R_L)$, is on the order of 1 k Ω . Using this value, it is estimated that the voltage drop at the junction V_j is a few percent of V_{ds} , corresponding to a few mV, because the total resistance of the sample is about 40 k Ω .

-
- [1] K. Novoselov, A. Geim, S. Morozov, D. Jiang, Y. Zhang, S. Dubonos, I. Grigorieva, and A. Firsov: *Science* **306** (2004) 666.
 - [2] K. Kuhn, C. Kenyon, A. Kornfeld, M. Liu, A. Maheshwari, W.-k. Shih, S. Sivakumar, G. Taylor, P. VanDerVoorn, and K. Zawadzki: *Intel Tech. J.* **12** (2008) 93.
 - [3] B. Huard, J. A. Sulpizio, N. Stander, K. Todd, B. Yang, and D. Goldhaber-Gordon: *Phys. Rev. Lett.* **98** (2007) 236803.
 - [4] R. V. Gorbachev, A. S. Mayorov, A. K. Savchenko, D. W. Horsell, and F. Guinea: *Nano Lett.* **8** (2008) 1995.
 - [5] A. F. Young and P. Kim: *Nat. Phys.* **5** (2009) 222.
 - [6] N. Stander, B. Huard, and D. Goldhaber-Gordon: *Phys. Rev. Lett.* **102** (2009) 026807.
 - [7] J. R. Williams, L. DiCarlo, and C. M. Marcus: *Science* **317** (2007) 638.
 - [8] B. Özyilmaz, P. Jarillo-Herrero, D. Efetov, D. A. Abanin, L. S. Levitov, and P. Kim: *Phys. Rev. Lett.* **99** (2007) 166804.
 - [9] S. M. Sze and K. K. Ng: *Physics of Semiconductor Devices* (Wiley-Interscience, New Jersey, 2006) 3rd ed., Chap. 8, pp. 417–465.
 - [10] L. Esaki: *Phys. Rev.* **109** (1958) 603.
 - [11] T. Yajima and L. Esaki: *J. Phys. Soc. Jpn.* **13** (1958) 1281.
 - [12] H. Miyazaki, S.-L. Li, A. Kanda, and K. Tsukagoshi: *Semicond. Sci. and Technol.* **25** (2010) 034008.
 - [13] E. McCann: *Phys. Rev. B* **74** (2006) 161403.
 - [14] T. Ando and M. Koshino: *J. Phys. Soc. Jpn.* **78** (2009) 034709.
 - [15] J. B. Oostinga, H. B. Heersche, X. Liu, A. F. Morpurgo, and L. M. K. Vandersypen: *Nat. Mater.* **7** (2008) 151.
 - [16] Y. Zhang, T.-T. Tang, C. Girit, Z. Hao, M. C. Martin, A. Zettl, M. F. Crommie, Y. R. Shen, and F. Wang: *Nature* **459** (2009) 820.
 - [17] K. F. Mak, C. H. Lui, J. Shan, and T. F. Heinz: *Phys. Rev. Lett.* **102** (2009) 256405.
 - [18] H. Miyazaki, K. Tsukagoshi, A. Kanda, M. Otani, and S. Okada: *Nano Lett.* **10** (2010) 3888.
 - [19] C. Sirtori: *Nature* **417** (2002) 132.
 - [20] V. Ryzhii and M. Ryzhii: *Phys. Rev. B* **79** (2009) 245311.

- [21] I. Meric, N. Baklitskaya, P. Kim, and K. Shepard: Electron Devices Meeting, 2008. IEDM 2008. IEEE International, dec. 2008, pp. 1–4.
- [22] H. Miyazaki, S. Odaka, T. Sato, S. Tanaka, H. Goto, A. Kanda, K. Tsukagoshi, Y. Ootuka, and Y. Aoyagi: Appl. Phys. Exp. **1** (2008) 034007.
- [23] Y. Yi, W. M. Choi, Y. H. Kim, J. W. Kim, and S. J. Kang: Appl. Phys. Lett. **98** (2011) 013505.
- [24] R. S. Bauer, R. Z. Bachrach, and L. J. Brillson: Appl. Phys. Lett. **37** (1980) 1006.
- [25] S. Roberts and P. J. Dobson: Jour. Phys. D: Appl. Phys. **14** (1981) L17.
- [26] S.-L. Li, H. Miyazaki, M. V. Lee, C. Liu, A. Kanda, and K. Tsukagoshi: Small **7** (2011) 1552.
- [27] S. R. Elliott: *Physics of Amorphous Materials* (Longman Scientific and Technical, Essex, 1990) 2nd ed.
- [28] J. Nilsson and A. H. Castro Neto: Phys. Rev. Lett. **98** (2007) 126801.
- [29] V. V. Mkhitarian and M. E. Raikh: Phys. Rev. B **78** (2008) 195409.
- [30] H. Min, D. S. L. Abergel, E. H. Hwang, and S. Das Sarma: Phys. Rev. B **84** (2011) 041406.
- [31] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, and P. Kim: Nat. Nanotech. **3** (2008) 654.
- [32] N. W. Ashcroft and N. D. Mermin: *Solid State Physics* (Brooks/Cole, Belmont, 1976), pp. 760–761.
- [33] M. Dresselhaus, G. Dresselhaus, and P. Eklund: *Science of Fullerenes and Carbon Nanotubes* (Academic Press (San Diego, California), 1996), Chap. 2, pp. 15–59.
- [34] F. Guinea, A. H. Castro Neto, and N. M. R. Peres: Phys. Rev. B **73** (2006) 245426.
- [35] B. J. van Wees, H. van Houten, C. W. J. Beenakker, J. G. Williamson, L. P. Kouwenhoven, D. van der Marel, and C. T. Foxon: Phys. Rev. Lett. **60** (1988) 848.

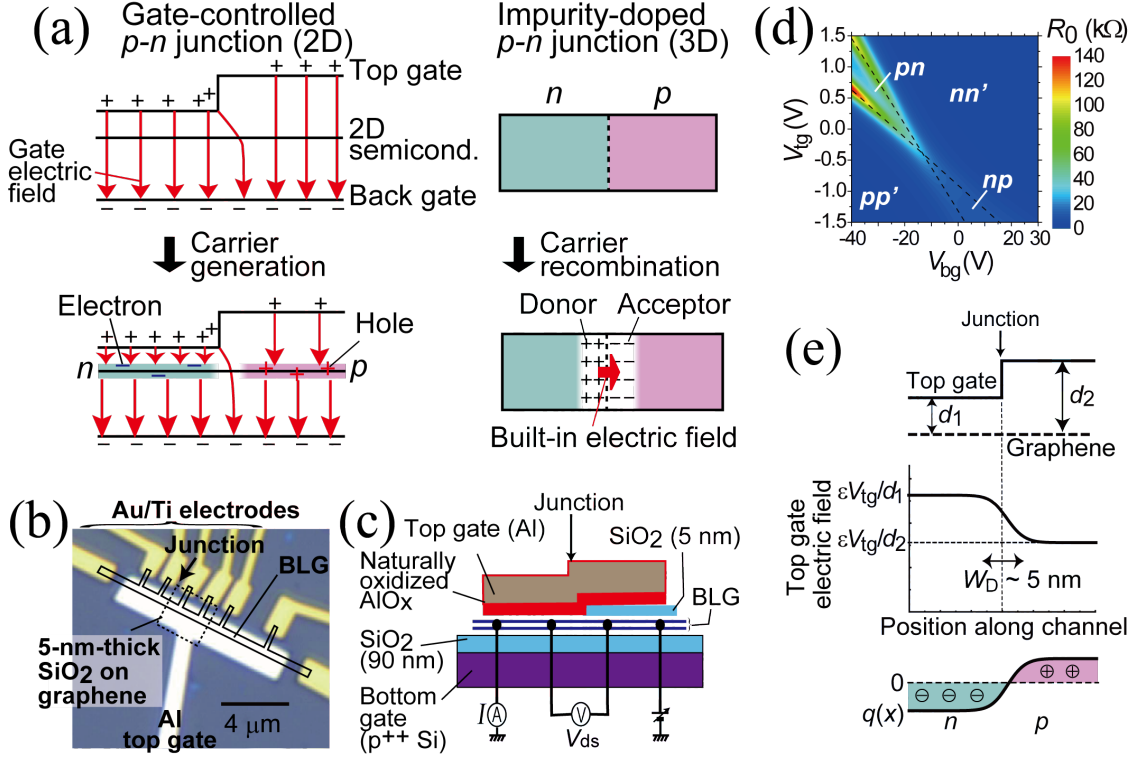


FIG. 1: (Color online) (a) Schematic diagram of p - n junction mechanism for a gate-controlled 2D semiconductor (left) and an impurity-doped 3D semiconductor (right). (b) Optical micrograph of a BLG p - n junction with a stepwise top gate. The solid lines show the shape of the graphene channel made by oxygen plasma etching. The dashed lines show the area in which the graphene is covered by a 5-nm-thick SiO₂ layer. (c) Schematic illustration of the cross-sectional view of the p - n junction. The locally inserted SiO₂ layer creates the stepwise structure in the top gate. The instrumental configuration for a four-terminal measurement is also shown. All transport properties shown in this paper were acquired in the same configuration. (d) Color map of the linear resistance, R_0 , as a function of V_{bg} and V_{tg} at $T = 80$ K, determined at $V_{ds} \sim 1$ mV. The dashed lines show the ridges of the CNPs separating p and n regions. (e) Schematic view of the geometrical structure of the stepwise top gate (top), the profile of the top gate electric field (middle), and the charge distribution (bottom). The top gate electric field is estimated numerically (Appendix A).

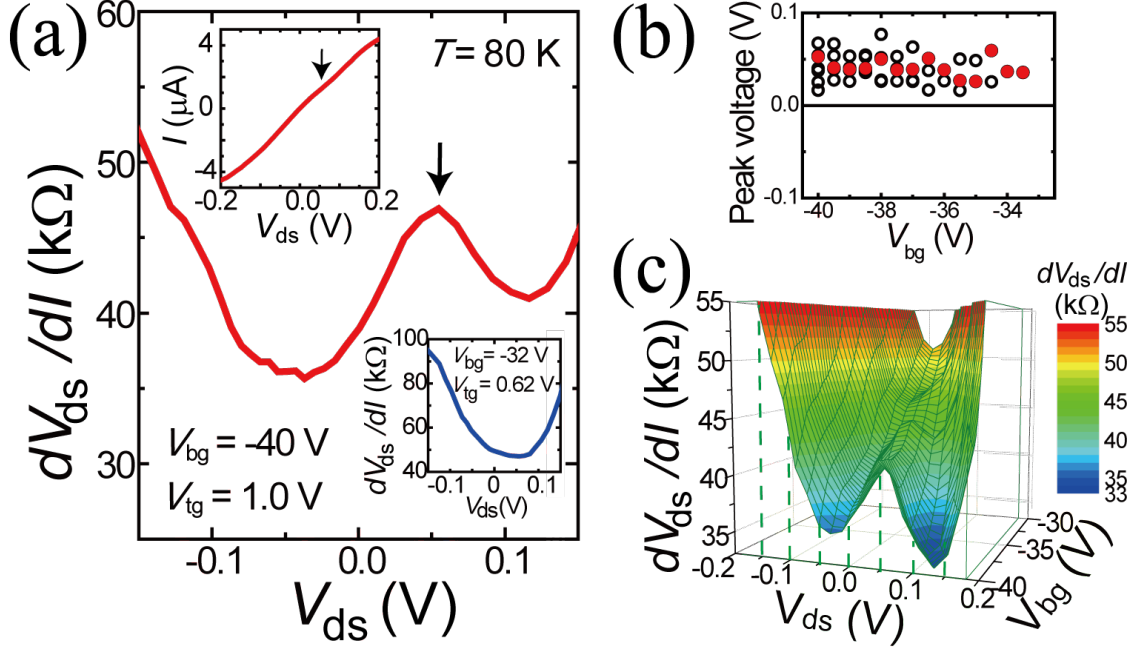


FIG. 2: (Color online) (a) Differential resistance, dV_{ds}/dI , as a function of the source-drain voltage V_{ds} for BLG under a relatively large electric field ($V_{bg} = -40$ V). The arrow indicates the dV_{ds}/dI peak. The top left inset shows current-voltage curve corresponding to the main panel. The bottom-right inset shows a dV_{ds}/dI - V_{ds} curve for a relatively small electric field ($V_{bg} = -32$ V). (b) Distribution of the V_{ds} values for the dV_{ds}/dI peaks as a function of V_{bg} with various values of V_{tg} . The red closed symbols correspond to the data shown in (c). (c) dV_{ds}/dI as a function of V_{ds} and V_{bg} . The V_{tg} value is selected along the middle point of two ridges of CNPs in Fig. 1(c). All data were acquired at $T = 80$ K.

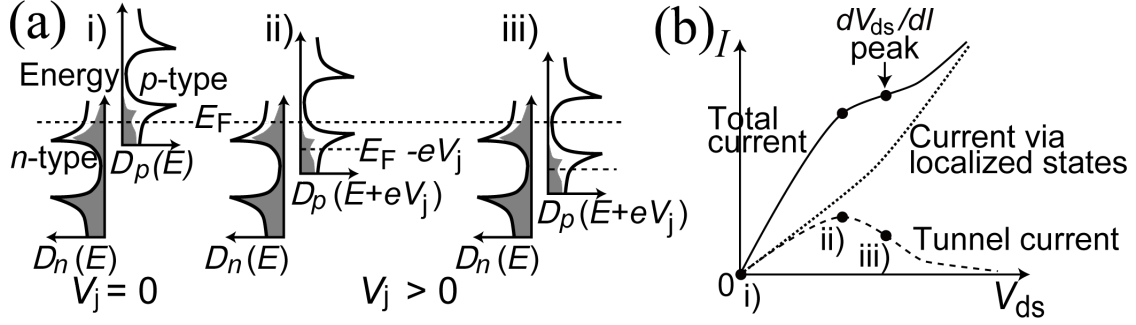


FIG. 3: (a) Schematic diagram of the DOS for the p -type and n -type sides: i) for the unbiased condition ($V_j = 0$) and ii)-iii) for the forward-biased ($V_j > 0$) conditions. The gray shaded areas show the density of occupied states with a Fermi distribution. Electron tunneling takes place from occupied states on one side to unoccupied states on the other side. (b) Schematic I - V_{ds} curve for the tunneling current (dashed curve), the current via localized states (dotted curve), and the total current (solid curve). The three conditions in (a) (i), ii), and iii)) are identified on the tunneling current curve and the total current curve.

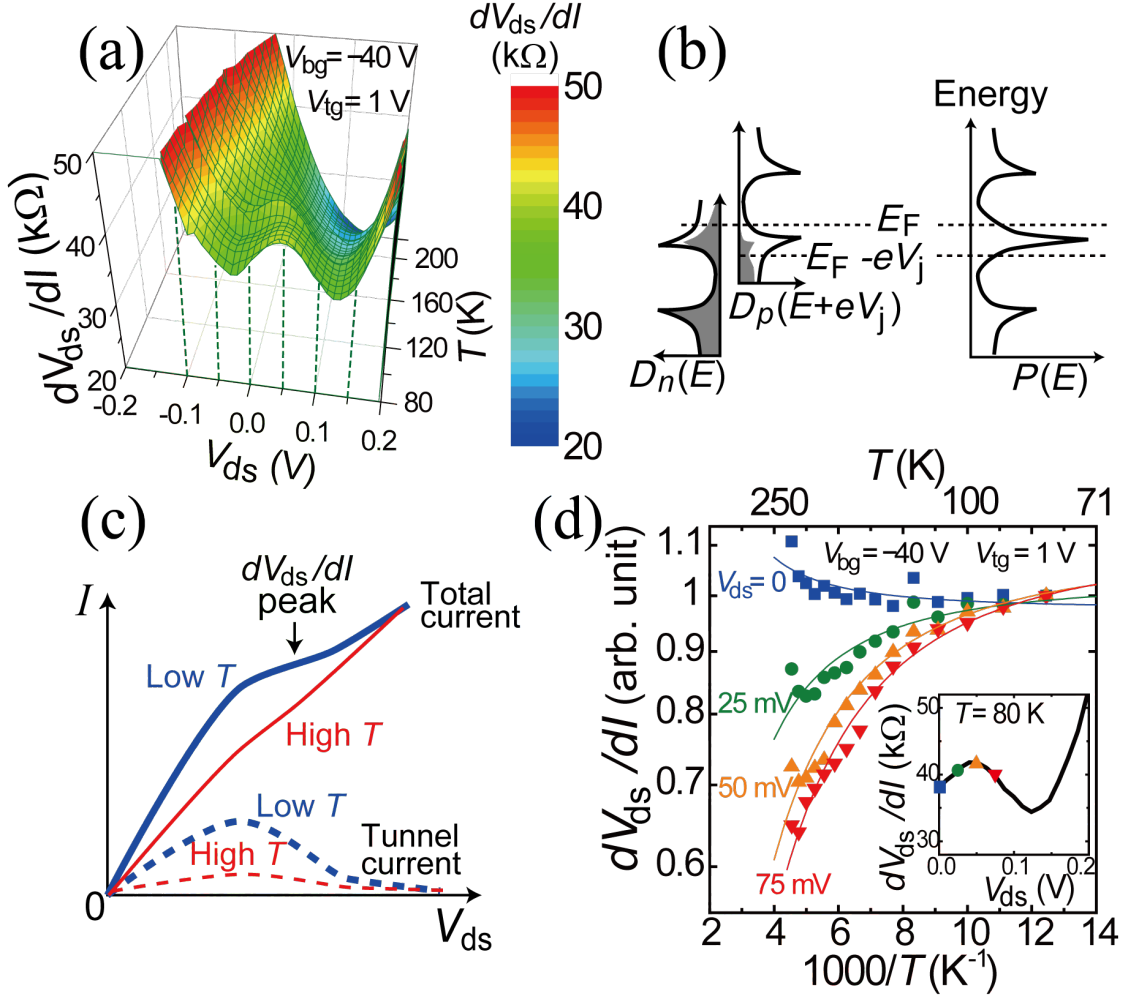


FIG. 4: (Color online) (a) Temperature dependence of the dV_{ds}/dI curve for $V_{bg} = -40$ V and $V_{tg} = 1.0$ V. (b) Schematic diagram of $A(E) = D_n(E)D_p(E + eV_j)$ under a forward voltage drop of V_j corresponding to the tunneling current peak (Fig. 3(a)ii). (c) Schematic current-voltage characteristics for the tunneling current at low temperature (thick dashed curve) and high temperature (thin dashed curve) and the total current with an additional leakage current (Fig. 3(b)) at low temperature (thick solid curve) and high temperature (thin solid curve). (d) Arrhenius plot of the dV_{ds}/dI values extracted from (a) at fixed values of V_{ds} for a forward bias ($V_{ds} > 0$). The dV_{ds}/dI values are normalized at $T = 80$ K. The solid lines represent fittings within second order of the temperature. The dV_{ds}/dI curve is shown for a forward bias at $T = 80$ K in the inset of (b), in which the markers indicate the corresponding V_{ds} values in the main panel.

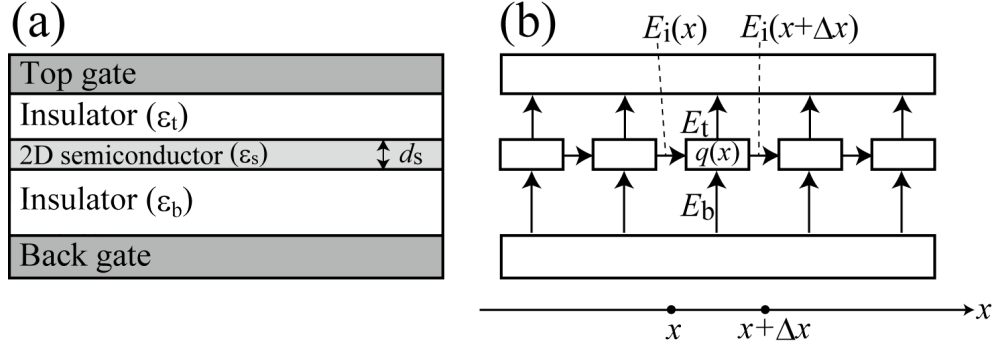


FIG. A.1: Schematic illustrations of (a) 2D semiconductor sandwiched between a top gate and a bottom gate and (b) electric field in the semiconductor plane (E_i) and in gate insulators (E_t and E_b)

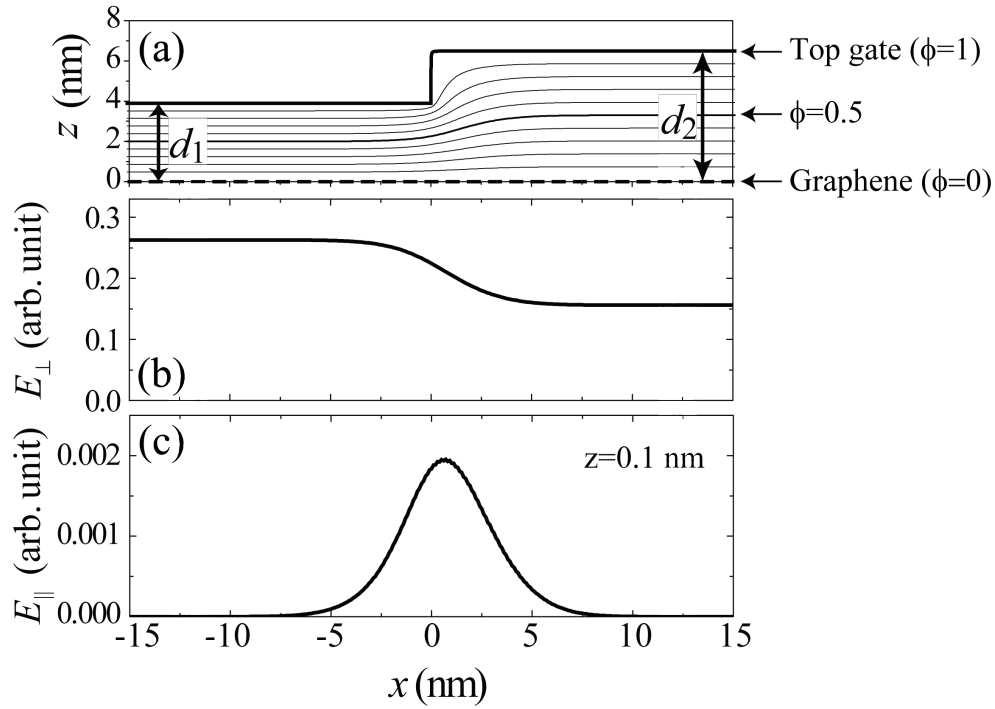


FIG. A.2: (a) Contour plot of electric potential ϕ with a boundary condition that $\phi = 0$ at the graphene and $\phi = 1$ at the stepwise top gate. The contour interval is 0.1. (b) Normal component of the electric field at the graphene surface. (c) Tangent component of the electric field at the vicinity of the graphene surface ($z = 0.1$ nm).

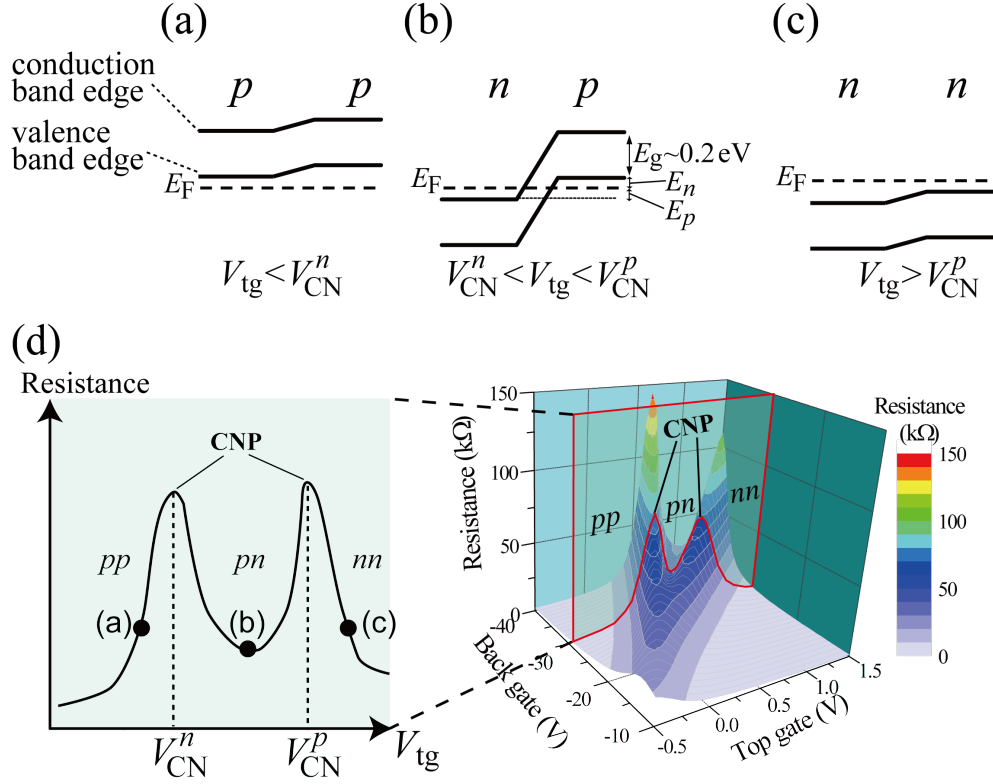


FIG. B.3: (Color online) Schematic band diagrams for combinations of (a) p - p , (b) n - p , and (c) n - n in the semiconductor graphene with the stepwise top gate. (d) The left panel shows resistance change as a function of the top gate voltage at fixed V_{bg} , and the right panel shows a 3D plot of the resistance as a function of the bottom gate and top gate voltage for the same data in the middle panel of Fig. 1(c). The left panel corresponds to the cross section in the right panel. The marked three points in the right panel correspond to the band diagrams (a)-(c).